# ELECTENG 101

## Electrical and Digital Systems

UNIVERSITY OF AUCKLAND · LEVEL 1 · SEMESTER 2, 2026

Full guide + ask Sia about ELECTENG 101

SIDE 1/2 EXAM MAP · CIRCUIT METHODS · SENSORS · OP-AMPS · DIGITAL · ADC · MOTORS

ONE A4 NOTE SHEET

Methods + assumptions + checks

## 0 · Exam Map

COURSE.JSON · CANVAS

Assignments 30% | IC | La | Tests 22% | Examination 40%

| ASSESSMENT | WEIGHT | FORMAT |
|---|---|---|
| Formative assignments | 30% | 10 weekly online |
| In-class exercises | 4% | 4 bi-weekly |
| Laboratory | 4% | 1, Week 10 or 11 |
| Tests | 22% | 2 × 11%, in person |
| **Examination** | **40%** | in person; restricted book/calculator |

"It is a restricted book (lite) and restricted calculator exam, which means you are allowed one double-sided A4 sheet of paper with anything you like written/printed on it." (ELECTENG 101 Examination page, Semester Two 2026 (Canvas))

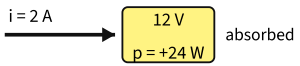
## 1 · Universal Solve Loop

CH 1 · GUIDE STRATEGY

| STEP | WRITE BEFORE ARITHMETIC | CHECK |
|---|---|---|
| 1 Label | nodes, current arrows, voltage polarities | same reference throughout |
| 2 Constrain | component law + topology law | units; open I=0, short V=0 |
| 3 Solve | signed equations | substitute into originals |
| 4 Interpret | magnitude, unit, physical direction | Σp=0; boundary sense |

**SIGNED QUANTITIES**

```
i = dq/dt  ·  v = Ri (passive references)
p = vi: p>0 absorbed; p<0 supplied
KCL: Σi at node = 0  ·  KVL: Σv around loop = 0
```




Passive convention: current enters + terminal, so 12 V × 2 A = +24 W absorbed.

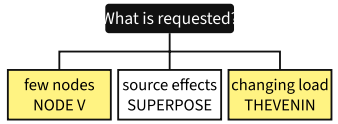
**EXAM →** *A negative answer usually reverses the chosen reference; it does not invalidate the equations. Keep the arrow, then translate the sign.*

**WHICH CONSERVATION LAW BITES?**

| CLUE | WRITE | DO NOT ASSUME |
|---|---|---|
| currents meet at one node | KCL with one entering/leaving convention | each branch current is positive |
| closed path with labelled polarities | KVL in traversal order | a "source" is automatically a rise |
| resistor current enters its + terminal | v=Ri and p=vi | negative result means failure |
| complete network power | sum signed element powers | magnitudes should be added |

## 2 · Choose the DC Method

CH 2 TOPIC MAP + FAQ




Choose by requested quantity: essential nodes, source contributions, or repeated load changes.

| METHOD | USE WHEN | PROCEDURE / BOUNDARY |
|---|---|---|
| Series/parallel | true shared current / true shared voltage | redraw nodes first; branching breaks series |
| Node voltage | few essential nodes, many parallel branches | choose reference; each branch $(V_a-V_\beta)/R$; one KCL per unknown node |
| Superposition | linear network, several independent sources | one source at a time; V-source→short, I-source→open; dependent sources stay; add signed V/I, never power |
| Thevenin | same network, changing external load | remove named load; Vth=Voc; find Rth looking in; preserve terminal polarity |

**REDUCTION AND DIVISION**

```
Series: Req = ΣR  ·  Parallel: 1/Req = Σ(1/R)
Divider across R2: V2 = VsR2/(R1+R2)
Thevenin load: I = Vth/(Rth+RL); VL = IRL
```

**NODE-VOLTAGE PATTERN**

```
At node a: Σ(Va-Vneighbour)/R = signed source current.
Diagonal collects attached conductances; other unknown-node terms enter with opposite sign. A source between two unknown nodes creates a supernode.
```

**THEVENIN RESISTANCE**

Deactivate **independent** sources only. If dependent sources remain or inspection fails, apply a test source at the named terminals and use `Rth=Vtest/Itest`. Endpoint checks: open circuit I=0 gives V=Vth; short circuit V=0 gives Isc=Vth/Rth.

**TRAP →** *An open-circuit load carries zero current; internal branches may still carry current. A terminal equivalent preserves load behaviour, not every internal branch current.*

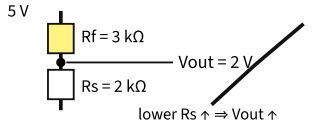
**SUPERPOSITION LEDGER**

1. Fix one reference direction for the requested response.
2. Keep one independent source active; set the others to zero using the correct open/short replacement.
3. Redraw topology after each replacement; retained resistors remain connected.
4. Calculate the signed contribution and repeat.

## 3 · Sensors → Voltage

CH 3 TOPIC MAP + FAQ

Separate the chain: measurand → sensor resistance → interface voltage → receiver. Predict the direction before calculating; it catches a swapped divider leg or output polarity.




Lower-leg sensor: Vout=VsRs/(Rf+Rs); increasing Rs raises the output.

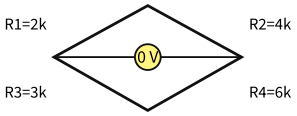
**DIVIDER INTERFACE**

```
Vout = VsRs/(Rf+Rs) when Rs is the lower leg.
Lower-leg Rs ↑ ⇒ Vout ↑. Upper-leg Rs ↑ ⇒ Vout ↓.
Sensitivity near an operating point = ΔVout/Δ(measurand).
```

**FINITE RECEIVER = LOADING**

```
Replace loaded lower leg: Rlower,eff = Rs ∥ Rin
R1∥R2 = R1R2/(R1+R2)
Then reapply divider; compare with open-circuit Vout.
```

| INTERFACE | WHAT IT PRESERVES / REVEALS | CHECK |
|---|---|---|
| Single divider | large baseline plus sensor change | position controls output trend |
| Bridge | difference of two midpoint voltages; small imbalance about a null | declare right−left or left−right |
| Buffer | divider voltage while supplying next stage | very high input R; low output R; gain ≈1 |




Bridge balance: R1·R4=R2·R3; equal midpoint ratios give zero differential output.

**BRIDGE METHOD**

```
Vleft = VsR3/(R1+R3)  ·  Vright = VsR4/(R2+R4)
Vout = declared midpoint subtraction.
At balance: R1R4=R2R3.
```

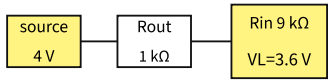
**EXAM →** *Calculate both midpoints to the same reference, then subtract in the stated order. Swapping leads changes sign, not imbalance magnitude.*

**INTERFACE AUDIT**

| STAGE | INPUT → OUTPUT | UNIT / BOUNDARY |
|---|---|---|
| sensor law | temperature, strain or light → resistance | physical units → Ω |
| divider/bridge | resistance → voltage | 0…Vs; declared polarity |

## 4 · Loading + Op-Amps

CH 4 TOPIC MAP + FAQ




Loading is a divider: a 4 V source, 1 kΩ output and 9 kΩ input deliver 3.6 V.

**SOURCE → RECEIVER**

```
VL = VsRin/(Rout+Rin). Good voltage interface: Rin ≫ Rout.
Buffer when the following stage materially changes the source voltage.
```

**IDEAL OP-AMP RULES—CONDITIONAL**

| RULE | USE ONLY WHEN | FAILURE CLUE |
|---|---|---|
| $i_+ = i_- = 0$ | ideal input model | loading belongs in external network |
| $v_+ \approx v_-$ | negative feedback and unsaturated output | open-loop/comparator or clipped output |
| Follower Vout≈Vin | negative feedback; within input/output limits | benefit is isolation, not gain |

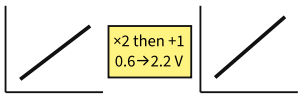
**CORE CLOSED-LOOP MAPS**

```
Inverting: Vout = -(Rf/Rin)Vin
Non-inverting: Vout = (1+Rf/Rg)Vin
Inverting sum: Vout = -RfΣ(Vk/Rk)
```

**AFFINE RANGE DESIGN**

For `Vout=aVin+b`, solve the two endpoint requirements first:

```
a=(Vout,2-Vout,1)/(Vin,2-Vin,1)
b=Vout,1-aVin,1
```




Gain sets slope; reference contribution sets offset. Check both endpoints and the rails.

**DIAGNOSIS ORDER**

1. **Loaded input:** did the receiver alter Vin?
2. **Feedback sign:** does output correction reduce the input difference?
3. **Rails:** is requested Vout physically reachable?
4. **Endpoint test:** minimum, midpoint and maximum input.

**TRAP →** *A correct symbolic gain can still demand an impossible output. Report ideal demand, violated rail and clipping; do not feed an impossible value into the next stage.*

**KCL BEFORE MEMORISED GAIN**

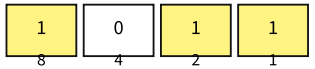
At a virtual summing node, write each resistor current from labelled endpoints and use zero ideal input current. A "virtual ground" is feedback-held near ground, not a wire that can source or sink arbitrary current.

## 5 · Number Systems

CH 5 TOPIC MAP + FAQ

**POSITIONAL VALUE**

```
(dn…d1d0)β = Σdibi. Keep base subscripts visible.
n bits ⇒ 2^n patterns; unsigned range 0…2^n-1.
Minimum width: smallest integer n with 2^n ≥ required states.
```




$1011_2 = 8+0+2+1 = 11_{10}$

Each digit earns its place value; binary $1011_2$ is decimal 11.

| TASK | METHOD | CHECK |
|---|---|---|
| Base b → decimal | expand weighted powers | digits must be <b |
| Decimal → base b | repeated division; read remainders last-to-first | re-expand |
| Binary ↔ hex | group from right in 4 bits; pad left only | leading zeros keep width, not value |
| Size field | test neighbouring powers of two | smaller fails; chosen width suffices |

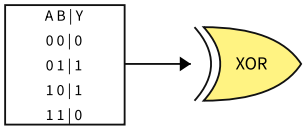
## 6 · Boolean Logic

CH 6 TOPIC MAP + FAQ

| A | B | AND AB | OR A + B | XOR A⊕B |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 | 0 |

**IDENTITY KIT**

```
A + 0=A; A·1=A; A + A=A; A·A=A
A + AB=A; A(A + B)=A
¬(AB)=¬A + ¬B  ·  ¬(A + B)=¬A¬B
```




Truth table, expression and gate must preserve the same decision for every row.

**FROM REQUIREMENT TO GATES**

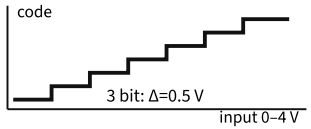
1. Define what 0 and 1 mean; mark active-low signals explicitly.
2. Enumerate all input rows.
3. For each output-1 row write its minterm: 1→variable, 0→complement.
4. OR the minterms; simplify one named identity at a time.
5. Rebuild the full truth table, especially adjacent boundary rows.

**GUIDE SAFETY-RULE DRILL**

## 7 · ADC Method

CH 7 TOPIC MAP + FAQ

Keep three decisions separate: **sampling** chooses times, **quantisation** chooses amplitude zones, and **encoding** assigns fixed-width binary codes.




Eight codes over 0–4 V give 0.5 V nominal steps; mapping convention fixes boundaries.

**UNIPOLAR N-BIT CONVERTER**

```
Ncodes=2^n  ·  Δ=(Vmax-Vmin)/2^n
For stated floor rule:
k=floor((Vin-Vmin)/Δ), clipped to 0…2^n-1.
Encode k in exactly n bits.
```

| SPECIFICATION CHANGE | IMPROVES | DOES NOT FIX |
|---|---|---|
| add one bit | twice the codes; half nominal Δ for fixed range | missed time variation |
| raise sampling rate | time resolution | amplitude step size |
| change reference range | range/headroom trade-off | code count |
| gain + offset | useful sensor span uses more codes | over-range tolerance unless headroom retained |

State the endpoint convention. Floor, nearest-level and centred-code maps differ at thresholds. Above/below range gives an endpoint code and loses the overdrive magnitude.

## 8 · DC Motor Response

CH 8 TOPIC MAP + FAQ




Electrical input divides into shaft output plus copper, magnetic, friction and windage losses.

**STEADY MOTOR EQUATIONS**

```
V = IaRa + Eβ  ·  τdev = ktIa
ω = 2π(rpm)/60  ·  Pshaft = τshaftω
Pin = VI  ·  η = Pshaft/Pin
```

| CHANGE | CAUSAL SEQUENCE |
|---|---|
| Start / stall | ω≈0 → $E_\beta$≈0 → $I_a$≈V/$R_a$, often large |
| Load torque ↑ | speed initially ↓ → $E_\beta$↓ → $I_a$↑ → developed torque ↑ → new operating point |
| Efficiency check | convert rpm; distinguish developed from shaft torque; output must not exceed input |

**BOUNDARY →** *Back emf is not a loss term; it links speed to armature current. If demanded torque exceeds motor/supply capability, the motor may stall.*



Your exam allows one A4 sheet of notes, both sides. Check on the LMS whether printed notes are accepted; if they must be handwritten, copy it.

Semester Two examination period, 29 October – 16 November 2026 (check your personal exam timetable).

# ELECTENG 101

## Worked Drills · Traps · Fast Recall

ELECTRICAL AND DIGITAL SYSTEMS · UNIVERSITY OF AUCKLAND

Full guide + ask Sia about ELECTENG 101

SIDE 2/2 FIVE WORKED DRILLS · AC POWER · TRANSFORMERS · METHOD CHOOSER · ERROR CLINIC

ONE A4 NOTE SHEET

Carry numbers to units + checks

### WE1 · Signed Two-Source Loop

CH 1 WORKED EXAMPLE

**Given:** 10 V source aids a clockwise current; 4 V source opposes it; 2 Ω and 4 Ω are in series.

**1 · PRESERVE CHOSEN DIRECTION**

KVL: 10 - 2i - 4i - 4 = 0

6 - 6i = 0 ⇒ i = 1 A clockwise

**2 · SIGNED SOURCE POWER**

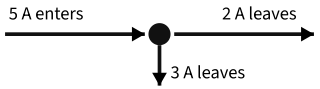
Current enters + terminal of 4 V source:

$p_4V$ = 4×1 = +4 W absorbed.

Resistors absorb: $1^2(2+4)$=6 W.

10 V source supplies 10 W.

| ELEMENT | ABSORBED POWER | INTERPRETATION |
|---|---|---|
| 2 Ω | 2 W | heat |
| 4 Ω | 4 W | heat |
| 4 V source | +4 W | receives energy |
| 10 V source | −10 W | supplies energy |
| **Σ** | **0 W** | balance |




KCL drill: 5 A in = 2 A + 3 A out; use one sign convention throughout.

**AUDIT MARKS**

- Labels survive into KVL.
- Source power follows terminal entry, not the source symbol.
- Every answer ends with magnitude, unit and direction.
- Reverse all references and the physical conclusion stays the same.

**TRAP →** *Do not "correct" a negative current by silently reversing its arrow halfway through the solution.*

### Quick Law Boundaries

CH 1 FAQ

| BOUNDARY | FORCED QUANTITY | NOT IMPLIED |
|---|---|---|
| open circuit | I=0 | V=0 |
| short circuit | V=0 | I=0 |
| DC steady capacitor | I=0 | stored voltage=0 |
| DC steady inductor | V=0 | current=0 |

**SIGN-ERROR CLINIC**

| SYMPTOM | CAUSE | REPAIR |
|---|---|---|
| current solves negative | physical direction opposes arrow | retain reference; state opposite direction |
| source "absorbs" unexpectedly | current enters its + terminal | use passive convention, not symbol type |

### WE2 · Recover the Hidden Source

CH 2 WORKED EXAMPLE

**Given terminal data:** (I,V) = (1 A,10 V) and (2 A,7 V). Assume the published linear terminal relation.

**1 · WRITE BOTH OPERATING POINTS**

V = Vth - IRth

10 = Vth - 1Rth

7 = Vth - 2Rth

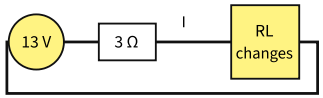
**2 · SUBTRACT, THEN BACK-SUBSTITUTE**

10-7 = (-Rth)-(-2Rth) ⇒ Rth=3 Ω

Vth = 10 + 1×3 = 13 V

**3 · ENDPOINT**

Isc = Vth/Rth = 13/3 = 4.33 A




Vth=13 V and Rth=3 Ω preserve the measured terminal line for any resistive load.

| POINT | I | V=13−3I | CHECK |
|---|---|---|---|
| open | 0 | 13 V | Voc=Vth |
| given 1 | 1 A | 10 V | matches |
| given 2 | 2 A | 7 V | matches |
| short | 4.33 A | 0 V | Isc=Vth/Rth |

**SOURCE SUPPRESSION RECALL**

| SOURCE SET TO ZERO | REPLACEMENT | MEANING |
|---|---|---|
| ideal voltage | short | 0 V enforced |
| ideal current | open | 0 A enforced |
| dependent | keep active | control remains |

**TRAP →** *Superposition adds signed current/voltage contributions. Compute power only from the recombined total: squaring creates cross-terms.*

### Method Cross-Check

CH 2 FAQ

For any proposed load point, verify it lies between open and short endpoints. A negative slope in the V–I terminal line corresponds to positive internal resistance under the stated current direction.

With a resistive load: I=Vth/(Rth+RL), VL=IRL.

As RL→∞: I→0 and VL→Vth.

As RL→0: VL→0 and I→Vth/Rth.

| EQUIVALENT STEP | EVIDENCE |
|---|---|
| name terminals + polarity | the later source orientation is fixed |
| remove only the named load | Voc is measured across the exposed pair |
| find Rth | independent sources at zero; dependent controls retained |
| reconnect load | calculated load V–I matches original network at those terminals |

**DEPENDENT-SOURCE CASE**

### WE3 · Loaded Sensor Divider

COURSE WORKED EXAMPLE

**Given:** 5 V supply; 3 kΩ fixed upper resistor; 2 kΩ lower sensor; 10 kΩ receiver loads the sensor.

**1 · COMBINE THE LOADED LOWER LEG**

Rlower = 2 kΩ ∥ 10 kΩ

= (2×10)/(2+10) kΩ = 1.667 kΩ

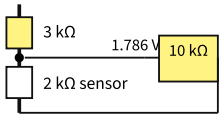
**2 · APPLY DIVIDER TO EFFECTIVE LEG**

Vreceived = 5×1.667/(3+1.667)

= 1.786 V

**3 · DIRECTION CHECK**

Unloaded Vout = 5×2/(3+2)=2.000 V. Receiver lowers the effective lower resistance, so 1.786 V < 2.000 V: correct direction.




Load is parallel with the 2 kΩ sensor before the divider calculation.

| QUANTITY | UNLOADED | LOADED | CHANGE |
|---|---|---|---|
| lower leg | 2 kΩ | 1.667 kΩ | decreases |
| output | 2.000 V | 1.786 V | decreases |

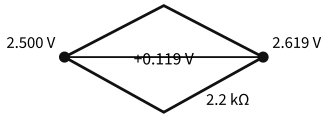
**BRIDGE EXTENSION FROM THE GUIDE**

A 5 V bridge starts with equal 2 kΩ arms. One lower sensor becomes 2.2 kΩ.

Both midpoints initially 2.5 V.

Changed midpoint = 5×2.2/(2+2.2)=2.619 V.

Right-left output = +0.119 V.




Calculate both midpoints to ground, then apply the declared right-minus-left polarity.

**TRAP →** *Do not insert the unloaded sensor resistance into the loaded divider. Do not report an unsigned bridge magnitude when polarity is stated.*

**SENSOR ANSWER CHECKLIST**

| BEFORE NUMBERS | AFTER NUMBERS |
|---|---|
| draw fixed/sensor positions and output polarity | does output rise/fall as predicted? |
| write the physical-input-to-resistance law separately | are physical and electrical units kept apart? |
| identify finite receiver resistance | was the parallel load combined first? |
| for bridge, label both midpoints to one reference | was subtraction performed in declared order? |
| decide whether a buffer is needed | is Rin high enough relative to source resistance? |

### WE4 · ADC Encode

CH 7 WORKED EXAMPLE

**Given:** ideal 4-bit ADC spanning 0–8 V; floor quantisation; Vin=5.3 V.

**1 · CODES AND STEP**

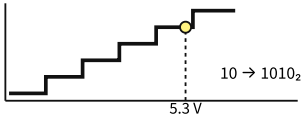
$2^4$=16 codes; Δ=8/16=0.5 V/code.

**2 · APPLY STATED MAP**

k=floor(5.3/0.5)=floor(10.6)=10.

**3 · FIXED-WIDTH ENCODE**

$10_{10}=1010_2$. Interval: 5.0 V ≤ Vin < 5.5 V.




Floor mapping sends 5.3 V to decimal code 10; binary output must contain four bits.

| BOUNDARY QUESTION | ANSWER DISCIPLINE |
|---|---|
| exact threshold | use the stated floor/round/centred convention |
| Vin<0 | clip to bottom code under stated saturating model |
| Vin>8 V | clip to 1111; overdrive amount is lost |
| more bits? | amplitude resolution only, not sampling rate |

**LINKED REPRESENTATION DRILL**

A device needs 700 states. Since $2^9$=512 is too small and $2^{10}$=1024 is enough, use **10 bits**; maximum unsigned value is **1023**. Also, $45_{10}=101101_2=2D_{16}$; at 10 bits write $0000101101_2$.

### Op-Amp Gain + Offset Drill

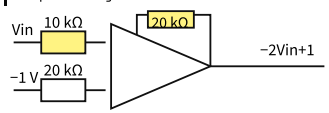
CH 4 WORKED EXAMPLE

Design Vout=-2Vin+1 V with Rf=20 kΩ and a −1 V reference input.

Rin=10 kΩ ⇒ -Rf/Rin=-2.

Rref=20 kΩ ⇒ -Rf(-1 V/Rref)=+1 V.

Therefore Vout=-2Vin+1 V; check endpoints against rails.




The resistor ratios implement the slope and reference contribution; rail checks remain mandatory.

**DIGITAL-BOUNDARY CLINIC**

| MISTAKE | CORRECTION |
|---|---|
| maximum written as $2^n$ | $2^n$ is pattern count; maximum is $2^n-1$ |
| minimum width rounded down | test the smaller power fails and chosen power suffices |
| remainders read top-to-bottom | first remainder is least-significant; reverse order |

### WE5 · Motor Operating Point

CH 8 WORKED EXAMPLE

**Given:** 24 V, 3 A, 1200 rpm, $R_a$=1 Ω, $k_t$=0.05 N·m/A, shaft torque 0.12 N·m.

**ELECTRICAL SIDE**

$E_b$=V-$I_aR_a$=24-3×1=21 V.

τdev=$k_tI_a$=0.05×3=0.15 N·m.

**MECHANICAL SIDE**

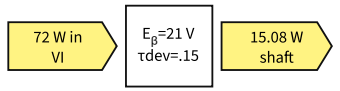
ω=2π(1200)/60=125.66 rad/s.

Pshaft=0.12×125.66=15.08 W.

**EFFICIENCY**

Pin=24×3=72 W.

η=15.08/72=20.9%.




Use developed torque for the electromagnetic relation and shaft torque for useful output.

**CHECK →** *Input exceeds output; rpm was converted before multiplying torque. At start, $E_b$≈0 and current is limited mainly by $R_a$.*

### AC Waveform Drill

CH 9 WORKED EXAMPLE

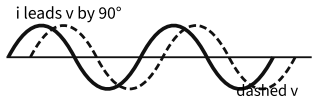
**Given:** C=20 μF and v(t)=10 cos(100t) V.

i=C dv/dt

=20×$10^{-6}$[-1000 sin(100t)]

=-0.02 sin(100t) A

=0.02 cos(100t+90°) A.




For a capacitor under passive references, current leads voltage by one quarter-cycle.

**AC RECALL**

x=Acos(ωt+φ); f=ω/(2π); T=2π/ω

sinusoid Xrms=Xpeak/√2

iC=C dv/dt; vL=L di/dt

S=VrmsIrms [VA]; P=S cosφ [W]; Q=S sinφ [var]

$P^2+Q^2=S^2$; pf=P/S=cosφ

| ELEMENT / LOAD | PHASE STATEMENT | DC STEADY LIMIT |
|---|---|---|
| capacitor | i leads v by 90° | open |
| inductor | i lags v by 90° | short |
| AC power | compare equal-frequency waveforms in same trig form | \|P\|≤S; \|pf\| ≤1 |

**POWER-FACTOR NUMERICAL CHECK**

The guide's load takes 4 A rms from 230 V rms at power factor 0.8 lagging:

S=230×4=920 VA.

P=S·pf=920×0.8=736 W.

|P|<S and |pf|<1: boundaries pass.

### Transformer + Grid Drill

CH 10 WORKED EXAMPLE

**Given:** ideal 20:1 transformer, Vp=4 kV rms, RL=10 Ω on the secondary.

**VOLTAGE FOLLOWS TURNS**

Vp/Vs=Np/Ns=20 ⇒ Vs=4000/20=200 V rms.

**CURRENT FOLLOWS INVERSE RATIO**

Is=Vs/RL=200/10=20 A rms.

Ip=Is/20=1 A rms.

**LOAD REFLECTION + POWER CHECK**

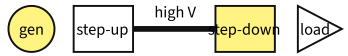
Rin=$(Np/Ns)^2$RL=$20^2$×10=4 kΩ.

VpIp=4 kVA; VsIs=4 kVA.




Ideal step-down: voltage ÷20, current ×20, apparent power unchanged, load reflects by $20^2$.

**GRID CHAIN AND LOSS LOGIC**




Raise voltage for transmission to lower current and $I^2R$ loss; reduce voltage near loads.

For fixed delivered real power and power factor: V↑ ⇒ I↓.

Line heating Ploss=$I^2R$: halving I gives one-quarter loss.

| BALANCED CONNECTION | LINE / PHASE RELATION |
|---|---|
| star | VL=√3Vph; IL=Iph |
| delta | VL=Vph; IL=√3Iph |

**Three-phase discipline:** label every value line or phase before selecting √3. Balanced formulas assume equal magnitudes and 120° displacement; do not multiply one phase by three for an unbalanced load.

Ideal-transformer VA equality omits winding, core, leakage, magnetising and regulation effects; it is a model assumption, not measured efficiency.

### Final Method Chooser

ALL TOPIC MAPS

| IF THE QUESTION ASKS… | START WITH… | LAST CHECK |
|---|---|---|
| branch/node value | references → Ohm + KCL/KVL | power balance |
| few essential nodes | node-voltage differences | original KCL |
| source contribution | superposition | add signed V/I only |
| variable load | Vth, Rth at named terminals | open/short endpoints |
| sensor chain | physical law → divider/bridge → loading | trend + polarity |
| op-amp map | feedback + KCL + endpoints | rails/loading |



Your exam allows one A4 sheet of notes, both sides. Check on the LMS whether printed notes are accepted; if they must be handwritten, copy it.

Semester Two examination period, 29 October – 16 November 2026 (check your personal exam timetable).